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SILICON MOLECULAR BEAM EPITAXY: 1984–1986

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Recent developments in the molecular beam growth of silicon and silicon compounds are reviewed including: techniques for substrate preparation and layer doping; heteroepitaxial growth of metal silicides, insulators and Ge_xSi_{1-x} strained layers; growth apparatus.

1. Introduction

This paper will provide a brief summary of recent studies on silicon molecular beam epitaxy (MBE). Work on the closely lattice matched materials, germanium silicide, nickel and cobalt disilicide and calcium fluoride, is also included. Discussion of GaAs on Si growth will be left to other authors in this volume. The paper includes sections on substrate preparation, doping, solid phase epitaxy, heteroepitaxial growth, and apparatus. Much of this work was presented in May 1985 in Toronto, Canada, at the first international meeting focusing on silicon MBE [1]. A second Si MBE symposium will be held in October 1987 [2].

2. Substrate preparation

The high quality and cost effectiveness of existing silicon material technologies place severe demands on an emerging process such as Si MBE. Although a number of substrate preparation procedures have proven adequate for research purposes, the challenge is to develop a simple, inexpensive technique that will yield consistent, uniform, large area silicon overgrowth with defect densities of less than $100/cm^2$. Recent work has concentrated in two areas: A re-examination of the established procedures of ex-situ chemical cleaning and in-situ sputter etching. And developments of new procedures such as UV ozone processing and in-situ reduction of surface oxides by silicon deposition.

It has been known for some time that a perfectly clean silicon surface has a strong affinity for carbon and that once formed these bonds are extremely hard to break [3]. Chemical cleaning procedures are, therefore, aimed at generating a passivating surface oxide layer rather than a clean silicon surface. These procedures generally employ hot basic or acidic peroxide solutions and go by the names RCA clean, Piranha etch, or Henderson etch. All yield a surface SiO_2 layer on the order of 10–30 Å thick. In early MBE work it was shown that these oxides can be removed in an MBE chamber at 800–900°C [4,5]. Residual carbon was then diffused away from the surface by a brief "flash" to ~1150°C. In 1982, Ishizaki et al. proposed a modified procedure that has been shown to yield a thin non-stoichiometric oxide [6]. This sub-oxide has an enhanced volatility and can be removed by vacuum anneals at 700°C. When preceded by multiple nitric acid baths, it was also claimed that carbon could be effectively eliminated. The stated 700°C requirement was critical in that at temperatures below ~800°C, silicon dopant diffusion and wafer deformation are absent.

The efficacy of the Ishizaki procedure has been closely examined by Xie et al. [7–9]. In contrast to earlier work, highly sensitive deep level transient spectroscopy (DLTS) and secondary ion mass spectrometry (SIMS) were used to examine

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epi/substrate boundaries. DLTS results indicate the existence of traps 0.58 and 0.59 eV below the conduction band edge. These traps persist in significant concentrations in substrates annealed at 700°C and decline to detection limits only after 950°C processing. SIMS data suggest a correlation with residual interfacial carbon that is presumably dispersed by the higher temperature anneal. If the need for 950°C processing is confirmed, this would reintroduce diffusion and deformation problems seriously undercutting the apparent advantage of the Ishizaki proposal.

Workers have also re-examined the early argon sputter cleaning and annealing procedure [10]. The sputter step is generally timed to remove ~ 100 Å of material within the MBE chamber. This is followed by an anneal of ~ 800°C to remove ion beam damage. The procedure has yielded the highest published MBE silicon minority carrier lifetimes of ~ 100 μs. Nevertheless, doubts persist about the possibility of residual ion beam damage.

Hull and co-workers have conducted a detailed examination of sputter cleaned epi/substrate interfaces using transmission electron microscopy (TEM) [11–13]. For certain samples, sputter times were shortened to produce removal of as little as 10 Å of material. It was thought that this would minimize ion beam damage and surface roughening, and might thus produce the highest quality interface. This was not the case. Longer sputter times produce interfaces and overgrowth free of observable defects. Shorter sputter times produce interfaces with small oxygen bubbles. It is apparent that ion bombardment knocks a small fraction of the surface oxygen deeper into the silicon. A number of atomic layers must thus be removed before this gradually decaying tail is eliminated. While this suggests the use of the longer sputtering times, the interfacial bubbles might be turned to advantage. Surprisingly, these bubbles did not nucleate threading dislocations in the overlying epi. As such, they might be employed as buried metal gettering centers.

A number of workers have recently proposed new or significantly modified sample preparation procedures. Kugimiya et al. [14,15] and Tatsumi et al. [16] have added in-situ silicon deposition steps to the chemical oxidation procedure. The aim was to enhance the removal of the protective oxide by using Si to reduce it to volatile silicon monoxide. This was done either by first coating the cool oxidized wafer with 5–20 Å of amorphous Si and heating or by heating the oxidized wafer under a low intensity silicon flux. Both procedures appeared effective and in particular, minimum annealing temperatures could be reduced to ~ 800°C and yet yield very low defect density (100) growth.

On the (111) orientation, Tatsumi et al. could not completely eliminate stacking faults. Building on the report of Tabe [17], an ozone chemical cleaning step was added. Tabe had shown a dramatic reduction in defect densities for both (100) and (111) wafers exposed to ozone (produced by UV illumination of air) and annealed in vacuum at $T > 900$°C. He speculated that the decrease was due to removal of residual carbon by ozone. Tatsumi et al. employed a modified procedure wherein ozone was formed by electric discharge of high purity oxygen gas and then bubbled into the wet chemical oxidizing solution. When combined with the above in-situ deposition of amorphous Si, he reported (100) growth with undetectable line and stacking fault densities, and (111) growth with line densities of 500–600/cm^2 and stacking faults of 800–900/cm^2.

On a related substrate preparation issue, Kubiak et al. have investigated the problem of boron spikes at MBE Si to substrate interfaces [18,19]. While these spikes are not believed to degrade crystallographic quality, they could greatly complicate the design of epitaxial devices. SIMS was used to measure spikes in samples prepared by a number of methods and handled according to different procedures. Typical areal boron concentrations of 10^{12}/cm^2 were observed. The presence of boron correlated most strongly with the air exposure of wafers. It was judged that particulates were not responsible and instead that boron was generated by outgassing of the wafer and interaction with chamber materials. The apparent problem source was the borosilicate glass viewports used on the MBE system. Substitution of quartz viewports reduced the boron level by a factor of 50. The quartz viewports still employ a borosilicate glass to metal seal, and it has been

learned that the near complete elimination of viewports has yielded a further boron reduction [20].

3. Doping processes

Doping has proven to be the single most difficult problem in silicon molecular beam epitaxy. On the basis of energy levels and solid solubilities, boron, arsenic and phosphorus are clearly the dopants of choice in the silicon materials system. Unfortunately, boron has an extremely high melting point (2300°C), making it difficult to generate sufficiently intense vapors without simultaneous outgassing from conventional evaporation cell materials. Arsenic and phosphorus go to the other extreme with vapor pressures so high that MBE systems are quickly contaminated to the point that background doping levels become unacceptable. Although gallium, aluminum and antimony have acceptable vapor pressures, very early MBE studies [4,21] showed that these species have strongly temperature dependent sticking probabilities and tendencies towards surface segregation. The remaining dopant, indium, was recently shown to have similar undesirable tendencies [22].

To overcome the above problems, recent work has focused on means of either cleanly sourcing boron or on implanting dopants a short distance below the growing epitaxial surface. Workers have taken two approaches to the sourcing of boron. The first, as described by Kubiak et al. [23,24], is the design of special high temperature Knudsen evaporation cells. These cells have not been described in detail but are known to pass electrical current directly through a graphite crucible (loaded with elemental boron) to produce temperatures of ~ 2000°C. The evaporated boron exhibits a temperature independent sticking probability (presumably unity) and doping profiles vary in a predictable manner with cell temperature. Comparison of $C-V$ and spreading resistance profiles indicates bulk carrier mobilities. On the question of possible contamination by cell outgassing, a critical examination of minority carrier properties and defect densities has yet to be reported.

A second approach to boron evaporation sourcing was recently reported by Ostrom and Allen [25]. They employed more conventional Knudsen cells in combination with molecular or alloy boron materials. In one experiment, B_2O_3 was evaporated congruently on heated silicon surfaces where it was hoped it would decompose releasing gaseous oxygen to the vacuum system and incorporating free boron. In a second experiment, silicon was melted in a boron nitride crucible to produce a boron saturated solution that was then used as a combined silicon and boron evaporation source. Both processes yielded controllable boron doping on the order of $10^{19}/cm^2$ with bulk carrier mobilities. SIMS measurements did not show enhanced oxygen incorporation with B_2O_3 sources. Again, critical minority carrier and defect studies have yet to be reported.

The balance of recent doping studies concerns means of overcoming surface re-evaporation and segregation problems by the use of low energy implantation. In a fairly conventional form, simultaneous low energy implantation doping has been used for some years [26–28], and has been shown to yield high quality doping with no need for post-growth damage annealing [29]. However, these studies employed complex and expensive bolt-on ion implantation systems with provisions for mass selection, focusing, beam raster scanning, and differential pumping. Recent work has been aimed at simplifying this process. In one set of experiments, Chrenko et al. [30] substituted a gallium liquid metal field emission ion source. This compact source could be mounted on a single flange directly on the MBE growth system. Because it employed no carrier plasma gas, mass selection and differential pumping could be deleted. In preliminary experiments, complex doping profiles were controllably generated to doping levels as high as $10^{19}/cm^2$.

Taking the simplification process one step further, Kubiak et al. [31–33] and Jorke et al. [34–36] have produced implantation-like doping by the mere application of a bias to the growing silicon sample. While there is not yet agreement on the incorporation mechanism, it is probable that silicon atoms, ionized by the electron beam evaporation source, are accelerated into that growing MBE surface. At the surface these ions collide with

accumulated surface layers of dopant knocking a fraction of these dopant atoms a short distance into the layer. Buried below the growing epi surface the dopants can no longer segregate or re-evaporate. This explanation is supported by Jorke's experiments showing a linear dependence of antimony incorporation with incoming silicon ion flux. While Kubiak does not rule out this secondary ion implantation mechanism, he suggests that experiments on bias dependence of incorporation might also be interpreted as evidence for an ion induced decomposition of complex surface dopant molecules into simpler, more readily incorporated species. Both groups have produced moderately well controlled, high level doping profiles. Kubiak reports bulk mobilities with no increase in etch pit densities.

In an intriguing recent report, Ennen et al. [37] discussed the use of erbium co-implantation doping to produce electro-luminescence from Si MBE layers. Light emission occurs as a result of internal 4f–4f electron transitions within the rare earth ion. The light is emitted in the 1.5 μm wavelength range favored for use with fiber optic communication links. The Si MBE layer serves only to support ions and to generate the pumping electrons by means of a forward bias p–n junction. External quantum efficiencies were estimated at $\sim 1\%$. While not intense by conventional LED standards, these experiments could open the door to a direct integration of light emitters on silicon based circuits.

4. Solid phase epitaxy

Solid phase epitaxy (SPE) involves the thermal recrystallization of amorphous films on a crystalline substrate. This process has been widely investigated and would normally fall beyond the scope of a review on MBE. In recent years, however, this process has been combined with conventional MBE to overcome the above problems of dopant incorporation. Doped amorphous layers are deposited on clean silicon substrates by co-evaporation of silicon and poorly behaved dopants such as antimony an gallium. It was hoped that during this room temperature process, dopants would lack sufficient energy to migrate or re-evaporate. This would eliminate the need for more complex high temperature Knudsen cells or ion beam sources. On the other hand, one must consider the possibilities that reduced temperatures will enhance contaminant incorporation and compromise crystalline quality.

The use of an MBE/SPE hybrid has been investigated by Streit, Metzger and Allen [38,39] and Casel et al. [40]. After room temperature deposition, doped amorphous layers are heated to temperatures of 530–630°C producing a recrystallization front moving up from the substrate with a velocity on the order of 1–10 Å/s. Streit et al. reported Ga and Sb doping levels as high as $10^{20}/cm^2$. At dopant concentrations of $\sim 10^{18}/cm^2$, n and p mobilities were measured at bulk levels. However, at both higher and lower doping concentrations, mobilities fell sharply to $\sim 50\%$ of accepted standards. Rutherford backscattering and channeling analysis suggested residual disorder near the epi/substrate interface. Hall effect measurements of Casel et al. also indicated a 30–50% reduction in p-type mobilities below bulk values. Detailed impurity and crystallographic analysis will be required to identify the degradation mechanism.

5. Heteroepitaxy: insulators

Towards the end of achieving three-dimensional integrated device structures, the epitaxial salts (Ca, Ba, Sr)F_2 have been investigated intensely since their original MBE synthesis by Farrow et al. [41] and Ishiwara and Asano [42]. Not only do these materials closely lattice match silicon, they have the attractive property of evaporating as stoichiometric molecules. Recent work has dealt primarily with the nature of the insulator/silicon interface and the improvement of crystallinity by post-growth processing.

These materials have the so-called CaF_2 lattice structure that is basically identical to that of silicon with the addition of four lattice sites. Despite this similarity, CaF_2 has been shown to grow with a 180° rotation from (111) Si substrates. The situation is further complicated by a multiplicity

of possible lattice terminations. Himpsel et al. have attempted to resolve the interfacial structure by use of high resolution core level spectroscopy [43]. These Si core level shifts are of opposite polarity depending on whether the interfacial Si atoms are bonded to Ca or F. In a complex series of arguments considering no less than six alternate interfacial geometries, Himpsel et al. conclude that data are most consistent with an interface wherein the final Si layer bilayer planes have the top Si row bonded to Ca atoms and the lower Si row to F.

Despite the relatively small mismatch between CaF_2 and Si (0.6% at 25°C), there have been persistent problems with crystalline quality. While the situation has been improved somewhat by optimization of growth conditions, one of the most promising strategies appears to be the post-growth application of rapid thermal annealing. As reported by Pfeiffer, Phillips et al. [44,45], CaF_2 on (100) Si has rather poor crystallinity for all growth temperatures but 600°C. At this temperature, crystallinity, while improved, is still substandard as indicated by a Rutherford backscattering minimum channeling yields of ~6%. The situation is drastically altered by 20s post-growth anneal at 1100°C. Low channeling yields are produced for samples grown over a 100°C substrate temperature range with the lowest channeling yields approaching the 3% value expected for defect-free material.

In a subsequent publication, Phillips and Augustyniak [46] applied rapid thermal annealing to $CaF_2/CoSi_2$/(111)Si structures. Prior to annealing, all growth temperatures yielded CaF_2 channeling minima of $\geqslant$ 20%. After rapid thermal processing, yields were lowered to 3–5% for a broad range of growth temperatures. Together these reports suggest an important role for such processing in those systems where lattice mismatch makes the complete avoidance of defects impossible.

In addition to these crystallographic studies, Smith et al. [47] have used epitaxial CaF_2 as the gate dielectric in a "metal epitaxial insulator semiconductor field effect transistor" (MEISFET). Transistor action was produced and the structure was used to measure breakdown field strength and interface state densities. These and other Si MBE device applications will be detailed in a companion review [48].

6. Epitaxial metals

The metal silicides $NiSi_2$ and $CoSi_2$ have the cubic calcium fluoride lattice structure with room temperature lattice mismatches to silicon of 0.4 and 1.2% respectively. They can be synthesized either by MBE co-deposition [49] or by metal deposition and thermal reaction [50]. Early work, on (111) silicon substrates, demonstrated a number of peculiar properties including multiple epitaxial relationships (0° and 180° rotations from the substrate) and the presence of small pinholes [51]. Subsequent work showed the advantage of predepositing 10–20 Å thick metal "template" layers to force one epitaxial relationship or to avoid breakup of (100) interfaces into (111) facets [52]. Recent work has been concerned with growth on other orientations, interfacial characterization, measurement of Schottky barrier heights and device application.

With mixed results, Tung et al. [53] have applied their "template" technique to metal silicide growth on (110) silicon. For one, they found that metal template thickness must be increased to 45–65 Å on this orientation to avoid discontinuous layers. These thicker template layers have decidedly poorer crystallinity than the thinner templates successfully employed on the (111) and (100) orientations. Additionally, the silicon to metal template interface has fine scale (111) facets producing a serrated interface with line defects at the peaks and valleys of the serrations. Nevertheless, subsequent deposition and reaction of thick $NiSi_2$ layers does produce high quality single crystal growth with Rutherford backscattering minimum channeling yields as low as 3%.

The suppression multiple metal silicide/silicon epitaxial relationships by metal templates is explained by Tung in the following manner [54]. Labeling the unrotated and 180° rotated interfaces type A and B respectively, Tung cites a body of experimental evidence that the type B interface has the lower intrinsic free energy. This

orientation will therefore be strongly favored when metal silicides are grown by near stoichiometric co-deposition or by reaction of a few monolayers of metal template layer. On the other hand, careful consideration of the layer stacking sequence shows that the movement of a type A $NiSi_2$/(111)Si interface requires rearrangement of a single layer of Si atoms and the diffusion of one atomic layer of Ni. The movement of the type B interface requires the simultaneous rearrangement of three atomic layers. Reaction of thick metal layers directly on Si will therefore involve a competition between type B nucleation and rapid type A propagation yielding local domains of both orientations. This competition is eliminated when predeposition of thin metal templates forces type B nucleation over the entire surface.

By templating and certain modifications of growth procedures, predominantly type A or B $NiSi_2$ growth can be produced on (111)Si. This has been exploited by Tung [55] and Hauenstein et al. [56] to study the nature of metal to silicon Schottky barriers. In general, metal/silicon Schottky barrier heights are surprisingly insensitive to interfacial orientation and composition. This could be due to interfacial contamination and imperfections, and to averaging over multiple metal grains of different orientation. These non-idealities are eliminated in the case of epitaxial metal silicides and, indeed, both groups report a clear orientation dependence of barrier heights. Tung and Hauenstein measured, respectively, barriers of 0.65 and 0.67 eV for type A interfaces versus 0.79 and 0.77 eV for type B. This clear and consistent dependence on fundamental interfacial properties should provide a long overdue means of discriminating between theories on barrier formation.

The relative perfection of metal silicide/silicon heterostructures has resurrected the two decade old idea of building a metal base transistor [48]. This structure is analogous to a conventional all semiconductor bipolar junction transistor but would overcome the series resistance problem inherent in narrow base structures. Both Rosencher et al. [57] and Hensel, Tung et al. [58,59] have reported transistor action in $Si/CoSi_2/Si$ structures although they disagree as to whether true metal base action is responsible. The dispute centers on the known tendency of epitaxial metal silicides to form small widely spaced pinholes that are filled with silicon when the layer is overgrown. These Si channels will create a parallel "permeable base transistor" action by the Schottky barrier depletion of carriers from the channels. Rosencher notes that he can observe two distinct transistor characteristics depending on silicide growth conditions [60], presumably due to either metal base or permeable base action. On the basis of computer simulations, Hensel counters that both modes can be produced by permeable base action [61]. Whatever the ultimate explanation, either mode may provide an attractive new device technology.

7. Ge_xSi_{1-x}/Si heterostructures

Until recently, there appeared to be no practical way of introducing semiconductor heterostructure capabilities to the silicon materials system. The few well lattice matched semiconductors come from the family of III–V materials and have thus far produced uncontrolled cross doping of adjacent silicon. In the Ge/Si system, Cullis and Booker [62] had shown that problems of lattice mismatch were compounded by a strong tendency towards three dimensional growth. Subsequent work by Kasper et al. [63,64] indicated that this islanding could be eliminated only for Ge_xSi_{1-x} alloys on Si with Ge fractions of $\leqslant 15$–20%. Unfortunately, data on bulk Ge_xSi_{1-x} showed that 15–20% alloys would have a bandgap only slightly below that of silicon [65].

In the last three years, several discoveries have radically altered the prospects of the Ge_xSi_{1-x}/Si system. For one, we have was shown that with careful substrate preparation, Ge_xSi_{1-x}/Si growth temperatures can be reduced from earlier minimum values of 700°C to below 500°C [66,67]. At these reduced temperatures, islanding problems are eliminated for all Ge fractions. Further, it was demonstrated that in the Ge_xSi_{1-x}/Si system, strained layer epitaxy can be maintained to thicknesses far beyond the limits predicted by earlier equilibrium theories [68,69]. Indeed, defect-free strained layer epitaxy can be maintained in dilute alloys to thicknesses of over one micron. In more

concentrated alloys, the critical thickness exceeds 10 Å for Ge fractions of up to 80%. This has facilitated the synthesis of useful superlattice structures [29,70] in which the cumulative defect-free alloy thickness is fifty times the predicted critical value for misfit dislocation formation.

In addition to facilitating defect-free growth, theory [71] and experiment [72] have shown that strain greatly reduces the Ge_xSi_{1-x} bandgap. For $x \geqslant 0.6$, the bandgap of strained Ge_xSi_{1-x} is actually smaller than that of pure bulk Ge [73]. Depending on the relative allocation of strain between the alloy and Si layers, these reductions in bandgap can produce either the so-called "Type I" or "Type II" heterostructure band alignments. With Type I alignment, the alloy bandgap falls between the Si bandedges and in the first Si modulation doping experiments this produced transfer of holes from doped Si to the adjacent alloy [74–76]. Subsequent experiments using symmetrically strained superlattices produced Type II alignment and transfer of electrons from doped Ge_xSi_{1-x} to undoped Si [77,78].

Exploiting the above properties, high quality silicon heterostructure devices have been fabricated on silicon with layer bandgaps 0.6 to 1.1 eV (at 25°C) [48]. These include p-modulation doped transistors [79,80], n-modulation doped transistors [81], 1.3 μm PIN [82,83] and SAM APD [84–86] photodetectors. Among the features of these experiments are the ability of the p-MODFET to successfully withstand conventional silicon planar processing, the demonstration of room temperature enhancement of electron mobilities in the n-MODFET, the APD detection of 1.3 μm light over 45 km optical links and the demonstration of gain bandwidth products of over 48 GHz.

Beyond these impressive early demonstrations of heterostructures silicon possibilities, there is intriguing evidence that strain may induce an atomically ordered state in Ge_xSi_{1-x} alloys. This was first suggested by electron diffraction experiments [87,88] interpreted as evidence for a (111) layer stacking sequence of GeGeSiSi. Subsequent X-ray diffraction data [89] supported the idea of ordering but did not directly confirm the suggested stacking sequence. Most recently, a close examination of Shubnikov–De Haas magnetoresistance power loss mechanisms has required the use of a dielectric loss term to fit experimental data [90]. The fit implies a dielectric constant 35% as large as that found in polar InAs. This would require a net non-random ordering of Ge–Si bonds. If these results are confirmed this would imply a Ge_xSi_{1-x} stained layer structure with a fundamentally altered crystal symmetry that could possess a range of properties normally excluded in diamond structure semiconductors.

8. Apparatus

In addition to the equipment features implicit in the above discussion, the last three years have seen a significant expansion in the commercial availability of equipment designed specifically for silicon MBE. Systems with 7.5–15 cm wafer capability are or will soon be available from VG Semicon, Riber, Physical Electronics, ANELVA and possibly Hitachi. At least one vendor, VG, will also supply add-on ion implantation doping equipment. These systems require less manual sample manipulation than earlier equipment and make increasing use of computer control. As has been the pattern for almost a decade in Si MBE, sample mounting requires no modification of standard wafers and direct radiant heating is used in place of III–V heater block and indium attachment schemes.

Despite the increase in wafer sizes, none of the above systems allows simultaneous deposition on multiple wafers. In contrast to many III–V device applications, the highly developed state of conventional silicon technology makes the add-on cost of Si MBE processing an extremely important consideration. Economic analysis suggests that it will be difficult if not impossible to reduce Si MBE costs to acceptable levels without a shift to multi-wafer processing [91,92]. Further, at even the device research level, the uniformity of simultaneous batch MBE processing would make it much easier to discriminate between variations caused by MBE and post-MBE processing steps.

Based on a Bell Labs design concept [93], a prototype batch processing MBE apparatus is being developed by VG Semicon. Using a unique

configuration of deposition sources and a flat rotating platen, it is calculated that this apparatus will achieve deposition uniformity of better than 5% for samples within ~ 0.22 meters of the platen axis. This would permit batch sizes ranging from fifteen 7.5 cm wafers to three 20 cm wafers. The demonstrated ability to grow Si MBE at rates as high as 1/3 μm per minute [28], means that deposition times may be as short as the periods required for sample loading, cleaning, cooling and unloading. The apparatus exploits this fact by dividing these functions between four in-line chambers allowing four batches to be in process simultaneously. It should thus ultimately be possible to attain throughputs as high as forty-five 7.5 cm to nine 20 cm wafers per hour. This apparatus is due to complete manufacturer's tests in late summer of 1986.

9. Summary

The last three years have seen a rapid expansion of Si MBE in terms of both fundamental capabilities and level of participation. By the time this review is published there may be as many as one hundred research groups active in the field. Work has centered in a number of areas. Sample preparation and layer doping continue to be actively investigated. While research capabilities exist in both areas, workers seek effective, simple and inexpensive alternatives. Heteroepitaxial capabilities have expanded radically during this period. A variety of epitaxial metal and insulators have been grown on silicon and work has begun on both detailed electrical characterization and device application. Ge_xSi_{1-x} strained layer epitaxy has at last added a viable semiconductor heterostructure capability to the silicon materials system. These alloys have demonstrated a number of unique strain induced properties and sophisticated device applications. Finally, problems of automation, throughput, and ultimate layer quality are being addressed as a variety of labs give serious consideration to the commercial application of Si MBE.

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